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Effect of changes to supply voltage and W/L ratio on full adder performance parameters

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ABSTRACT: In this article we analyse the effect to changes the supply voltage and W/L ratio on the propagation delay and total power consumption of 8T based full adder cell. There are many parameters which directly or indirectly affected the propagation delay of CMOS circuit. Supply voltage, transistor sizing, equivalent resistance, load capacitance and switching threshold are the parameters which affected the value of transistor parameters. But there is a trade off between all these parameters. So, designer have to take care with handling these parameters.

I. INTRODUCTION

This article contributes to a better understanding PDP minimization of single-bit 8T full adder cells when low power, high speed, less leakage and high performance are critical. Full Adder cell based on 8 transistor have been implemented in H-SPICE suit and simulated using 45 nm CMOS technology to obtain the performance of the cells with respect to minimal power dissipation. In this work, we studied single-bit 8T full adder. We have analyze the all the adder in terms of power and delay. The analysis has been carried out in different supply voltages. We changes the supply voltage and measure the changes in delay and power. Fig. 1 show the proposed 8T based full adder cell.

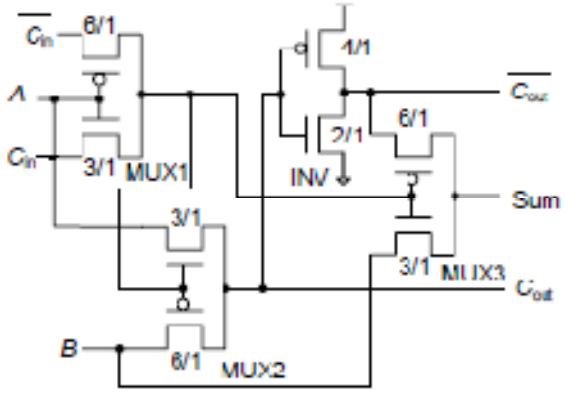

Fig. 1. The proposed eight transistor full adder (8T).

This proposed circuit is very special because of the propagation delay of this circuit. We find the lowest delay through this circuit. All simulated value of this circuit is given in the end of this chapter. And all the parameters affected this circuit also analysed in this paper, the results are shown below.

II. SIMULATED WAVEFORM OF 8T BASED FULL ADDER CELL

Simulated results of the given circuit is shown in figure B. For high inputs all the outputs like sum and carry are high and for low inputs all the outputs are low, which shows the functioning of full adder cell.

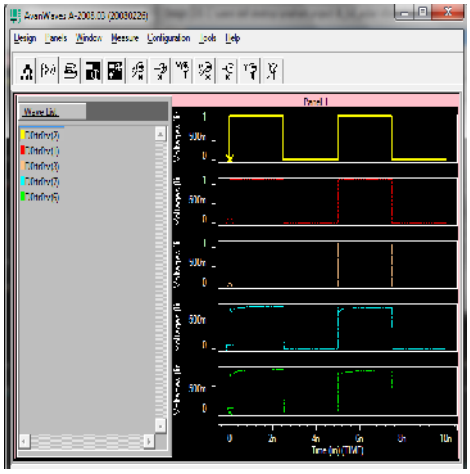

Fig. 2. Simulated waveform of 8T based full adder cell.

H-SPICE are the most powerful and effective performance optimization tool in the hands of the designers. This circuit simulate on the H-SPICE tool. Proceeded however with cautions when apply this approach. Increase the transistor sizes also raise the diffusion capacitances and hence C_L. In fact, once the intrinsic capacitances (i.e. the diffusion capacitances) start to dominates the extrinsic load form by wiring and fanout, increase the gate size do not longer help in reducing the delay, and only make the gates larger in area. These effects are called "self-loading". In addition, wide transistor has a larger gate capacitances, which increase the fan-out factors of the driving gate and adversely affect its speed. The relation between W/L and delay given in equation 1 and 2 for nMOS and pMOS respectively.

$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\mu_n C_{ox}(V_{DD}-V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD}-V_{T,n}}+\ln\left(\frac{4(V_{DD}-V_{T,n})}{V_{DD}}\right)-1\right] \quad \ldots(1)$$

$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\mu_p C_{ox}(V_{DD}-|V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD}-|V_{T,p}|}+\ln\left(\frac{4(V_{DD}-|V_{T,p}|)}{V_{DD}}\right)-1\right] \quad \ldots(2)$$

According to the above equation, the relation between transistor ratio and delay is shown in this chapter. This is very important to know that, how the transistor ratio affected the value of delay. We can see that by increasing the width of transistor or by increasing the transistor ratio, delay is going to reduce. It is also clear from the equation 1 and 2. But we can not increasing the width of transistor after a range (which depend on the load capacitance) because by further increasing the width over delay is not going to decrease or it may be increase after a range.

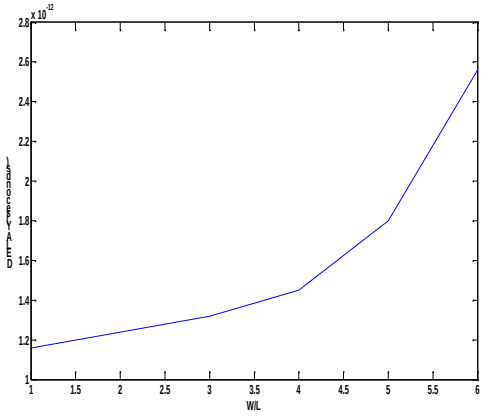

Fig. 3. Graph between W/L ratio vs Propagation delay

III. INCREASE V_{DD}

As illustrated above, the delay of a gate may be modulate by modify the supply voltages. This flexibility allow the designer to trade-off energy dissipations for performance, as we will seeing in a previous section. However, increase the supply voltage above a certain level yield only very minimal improvements and hence should be avoid. Also, reliability concern (oxide breakdown, hot-electrons effect) enforce firm upper-bound on the supply voltages in deep sub-micron process.

We knows that continuing technology scaling forces the supply voltage to reduces at rate similar to the devices dimension. On the same time, device threshold voltage is virtually keep constant. The readers probably wonder about the impact of this trend on the integrity parameter of the CMOS circuit. Does circuit keeps on working when the voltage is scaled and is there potential limit to the supply scaling?

A first hint on what might happen was offered in Eq. (3) which indicates that the gain of the inverter in the transition region actually increases with a reduction of the supply voltage!

$$g=-\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn}+k_p V_{DSATp}}{\lambda_n-\lambda_p}$$

$$\approx\frac{1+r}{(V_M-V_{Tn}-V_{DSATn}/2)(\lambda_n-\lambda_p)} \quad \ldots(3)$$

Where r is the transistor ratio, V_M is switching threshold voltage, V_{Tn} is the threshold voltage for nMOS.

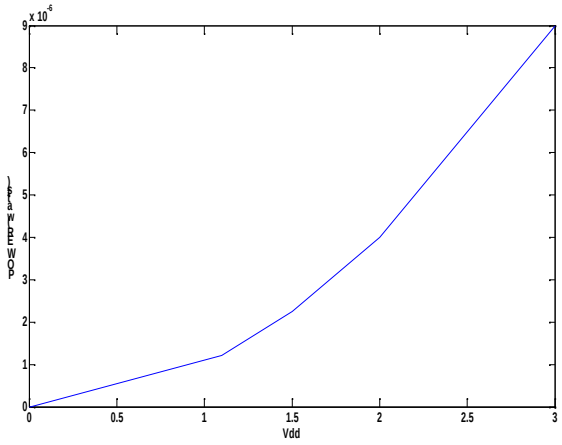

Fig. 4. Effect of changes to supply voltage on Power consumption.

λ_n and λ_p are the channel length modulation for the nMOS and pMOS respectively. V_{DSATn} is the saturation voltage for the nMOS.

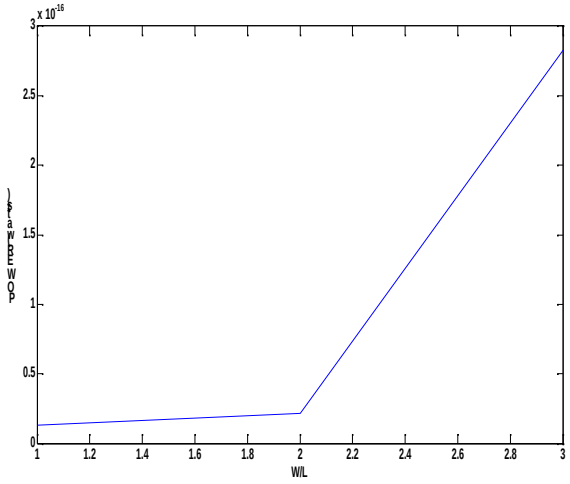

Fig. 5. Effect of changing the W/L ratio on power consumption.

IV. CONCLUSION

The performances of digital VLSI applications depend largely on the characteristic of the full adder circuit employ in such system. The novel full adders design propose are composed of only eight transistor forming three multiplexer and one inverter to produces complementary carry signal and summation signals. This paper include the effect of change in the value of supply voltage and transistor sizing on delay and power. By this analysis we can observe a value of supply voltage and transistor width on which we can find minimum power and delay. We can also set a trade off with the help of this analysis.

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